REMARKS

Claims 5-6, 9-11, and 28 are cancelled. Claims 1-4, 7-8, 12-27, and 29-32 are pending. Claims 1, 2, 12, 13, 15, 16, 18, 21, 24, 29, 30, 31, and 32 have been amended.

Applicant wishes to thank Examiner Li and Supervisory Examiner Kim for holding a personal interview with Applicant's Attorney on October 30, 2003. Applicant also appreciates the Examiner's willingness to conduct telephone interviews during February 2004 with Examiner Anderson. The discussions were very helpful. Information from the interviews is being used as the basis for this response.

In the Office Action mailed November 20, 2003, the Examiner objected to claim 29. The Examiner rejected claims 15-18 under 35 U.S.C. §112, second paragraph for indefiniteness. The Examiner rejected claims 1-2, 19, 28, and 31 under 35 U.S.C. §102(b) as anticipated by U.S. Patent No. 5,956,746 to Wang (hereinafter "Wang").

The Examiner rejected claims 3-4, and 22-23 under 35 U.S.C. §103(a) as obvious in view of Wang and U.S. Patent No. 5,325,504 to Tipley et al. (hereinafter "Tipley"). The Examiner rejected claim 7 under 35 U.S.C. §103(a) as obvious in view of Wang and Japanese Patent No. 404367954 to Kurkawa (hereinafter "Kurkawa"). The Examiner rejected claim 8 under 35 U.S.C. §103(a) as obvious in view of Wang and U.S. Patent No. 5,606,688 to McNutt (hereinafter "McNutt"). The Examiner rejected claims 11-14 and 25-27 under 35 U.S.C. §103(a) as obvious in view of Wang and U.S. Patent No. 4,490,782 to Dixion (hereinafter "Dixion"). The Examiner rejected claims 15-18 under 35 U.S.C. §103(a) as obvious in view of Wang and U.S. Patent No. 6,453,389 to Weinberger (hereinafter "Weinberger"). The Examiner rejected claims 21, 29-30 and 32 under 35 U.S.C. §103(a) as obvious in view of Wang.

Applicant has amended claims 1, 2, 12, 13, 15, 16, 18, 21, 24, 29, 30, 31, and 32 to clarify the invention and to comply with the objections of the Examiner.

REJECTION OF CLAIMS 15-18 UNDER 35 U.S.C. §112, 2nd paragraph

The Examiner rejected claims 15-18 under 35 U.S.C. §112, 2nd paragraph for indefiniteness. Applicant has amended claims 1, 15, 16, and 18 to address the antecedent basis

concerns raised by the Examiner. Applicant asserts that these amendments make claims 15-18 definite. Applicant requests that this rejection be withdrawn.

REJECTION OF CLAIMS 1-2, 19, 28, and 31 UNDER 35 U.S.C. §102(b) IN VIEW OF WANG

The Examiner rejected claims 1-2, 19, 28, and 31 under 35 U.S.C. §102(b) in view of Wang. Applicant respectfully traverses this rejection.

Anticipation under 35 U.S.C §102(b) requires that each and every element of the claimed invention be disclosed in the prior art. *Akzo N.V. v. United States International Trade Commission*, 1 USPQ 2d 1241, 1245 (Fed Cir. 1986). Further, anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *W.L. Gore & Associates v. Garlock, Inc.*, 220 USPQ 303, 313 (Fed Cir. 1983). Applicant respectfully asserts that every element of the present invention is not disclosed in a single prior art reference. In particular, Wang does not disclose prefetching of data elements into a cache. In addition, Wang does not disclose assigning of priority values to modeled data elements are recited in amended claim1.

Although the prefetching element is clearly set forth in claim 2, in order to advance prosecution, Applicants have amended claim 1 to include execution of prefetches scheduled based on modeled data elements in the model. The specification supports this amendment: "the prefetch scheduling system may selectively prestage data elements into the LRU cache." (Page 5, line 22).

In the art there is a distinction between fetch and prefetch. A fetch is issued to get information that is currently required by a CPU. The CPU has requested data or an instruction for a specific memory address. Prefetch is not the act of filling the cache under standard cache theory. A standard cache is filled when the CPU requests data that is not located in the cache. At that point, the CPU fetches the data from memory and the data is stored in the cache.

A prefetch is issued to get information that **may** be needed in the future and is not based on a specific memory request from the CPU. The prefetch is based on historical information but not on any particular memory request from the CPU. One example of such historical information

is the hit ratio. Applicants respectfully assert that one of the only reasons to consider the hit ratio of prefetched data compared to other data elements in the cache is that the prefetched data was loaded into cache based on an anticipated need rather than on a cache miss as occurs in the prior art. The distinction between fetching and prefetching is supported in the specification. (Page 12, line 27 - Page 13, line 7). This illustrates that prefetches are executed to load data from memory which has not been requested by a CPU, but which is anticipated to be needed.

In view of the telephone interview, the Examiner asserts that Wang teaches and discloses prefetching of data elements into the cache as recited in amended claim 1. The Examiner relies on Col. 5, line 66 through Col. 6, line 27 and Figures 3, 5, and 6 of Wang as teaching "prefetching" data from the BSRAM array 24 into storage 106. Applicants respectfully disagree.

Applicants assert that Wang as a whole does not perform any prefetching. There is no loading of data into cache in anticipation that the data will be needed in the future by the CPU. Instead, Wang teaches fetching of data both into the main cache 24 and into the storage buffer 106.

In particular, the sections of Wang relied upon by the Examiner also do not teach prefetching. This section begins by discussing how the predictor 54 in Wang functions. *Wang* Col. 5, lines 45-49. Please note that use of the predictor 54 is contingent on the CPU placing a requested memory address in the address register 64. In other words, the CPU has requested data from a specific memory location. In response to this memory request, Wang explains how his tag comparison of certain bits of the address and loading of tags and portions (half chunks) of data elements into the four ways of the cache 24 allow this request to be fulfilled. *Wang* Col. 5, line 50 through Col. 6 line 7.

Next, Wang describes how the half-chunks of data C0-A, C0-B, C3-A, C1-A, C1-B, C3-B, C2-A and C2-B are moved into the storage buffer 106. *Wang* Col. 6 line 7. Wang refers to Figure 6 to illustrate that his method fetches more data chunks per clock cycle than the prior art. Consequently, Wang load, or fetches four data elements (C0-A-C0-B, C1-A-C1-B, C3-A-C3-B, and C2-A-C2-B) from the cache 24 in three clock cycles. However, none of these data elements are being fetched in anticipation of being needed in the future. Therefore, this is not a prefetch operation. Instead, four candidate data elements are fetched and then compared with the

requested memory address to determine if the requested data element is in the cache 24. If so, "the desired cache line formed of the half-chunks in storage 106 is available [to the CPU]." *Wang* Col. 6, line 21-22. The desired cache line is C0, C1, C2, or C3. *Wang* Col. 4, line 40-45.

Wang does not discuss what happens to the remaining three cache lines. Presumably, these cache lines are flushed from the storage buffer 106. Wang clearly does not teach that these cache line data elements are retained in the storage 106 in anticipation of a future need of the cache lines by the CPU. Instead, Wang indicates that the process of loading four cache lines into storage 106 is repeated for a subsequent CPU request which would overwrite any previous cache lines left in the storage 106.

The predictor 54 in Wang also does not prefetch data in anticipation of future need by the CPU. Rather, the predictor is a determinative set of circuitry which decodes a portion of the address from a memory request and assists in searching a cache to find data already present in the cache. Wang uses the predictor to increase the efficiency of a 4-way set-associative cache by predicting which of the four ways will contain the desired data.

Therefore, because Wang fails to teach or describe prefetching of data as recited in amended claim 1, Applicants assert that claim 1 is in condition for allowance over the prior art of record.

In addition claim 1, has been amended to further clarify and emphasize that modeled data elements are assigned priority values. Cache management decisions are made based on the priority of modeled data elements and the priorities assigned to requested data elements. These elements are found in allowed claim 20. The priorities are based at least in part on whether data elements logically preceding the requested data element are already in the cache. This means that the requested data element is more likely a sequential data element in memory. Data elements ahead of this requested data element in memory have already been requested. Consequently, subsequent data elements are more likely to be requested in the future. In such a circumstance, the present invention may schedule a prefetch for subsequent data elements.

Applicants have amended independent claims 21 and 29-32 (referred to herein as "independent claims") to include substantially the same elements as those added in claim 1. Namely, these independent claims recite prefetching of data based on the history of data elements

in the model and assignment of priorities based on location information for the data elements. Dependent claims 2, 19, and 31 depend from these independent claims. Therefore, Applicants respectfully assert that these dependent claims are allowable for at least the same reasons as claim 1.

REJECTION OF CLAIMS 3-4, 7, 8, 11-18, 25-27, 21, 29-30, and 32 UNDER 35 U.S.C. §103(a) IN VIEW OF WANG AND OTHER PRIOR ART REFERENCES

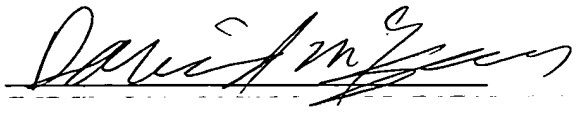
The Examiner rejected claims 3-4, 7, 8, 11-18, 25-27, 21, 29-30, and 32 under 35 U.S.C. §103(a) principally in view of Wang. The addition, the Examiner relied on Wang in combination with Tipley, Kurkawa, McNutt, Dixion, and Weinberger (referred to herein as "other prior art references"). Applicant respectfully traverses this rejection.

To establish a *prima facie* case of obviousness, the combination of the prior art references must teach or suggest all the claim limitations. *See* MPEP § 2142. Applicants assert that a *prima facie* case of obviousness has not been made because, as discussed above, Wang fails to teach or disclose prefetching of data elements into the cache or assignment of priorities to data elements in a model based on the history of the data element in the cache. The other prior art references also fail to teach at least these two aspects of the present invention.

Claims 5-6, 9-11, and 28 have been cancelled. Claims 3-4, 7, 8, 12-18, 25-27, 21, 29-30, and 32 depend directly or indirectly from the independent claims. For the reasons explained above, Applicants respectfully assert that the amended independent claims are allowable in view of Wang and the other prior art references. Therefore, Applicants respectfully assert that claims 3-4, 7, 8, 12-18, 25-27, 21, 29-30, and 32 are allowable for at least the same reasons as the independent claims.

In view of the foregoing, Applicant submits that the application is in condition for immediate allowance. In the event any questions remain, the Examiner is respectfully requested to initiate a telephone conference with the undersigned.

Respectfully submitted,



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